**EXPERIMENT - 1**

**AIM: Realize all gates by verifying their truth tables.**

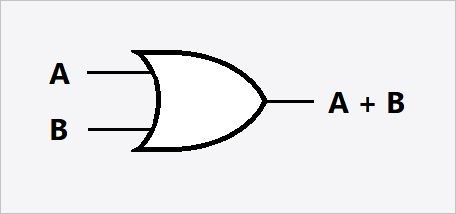
**HARDWARE REQUIRED: Power supply/ Voltage supply, Bread Board, Resistors, LEDs, Connecting Wires, Integrated Chips ICs (7404, 7408, 7432, 7486, 7400, 7402, 74266)**

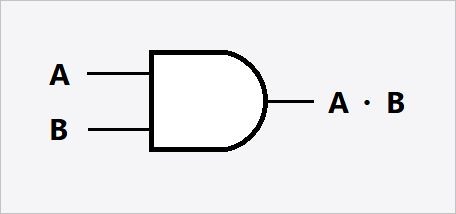
**SOFTWARE REQUIRED:**

**Software stimulator (MULTISIM) –** [**www.multisim.com**](http://www.multisim.com) **(free software) Stimulating schematic models of desired circuits**

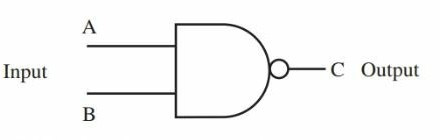
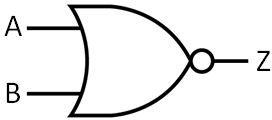
**Components used – Source (Clock Voltage), Passive elements (resistor), Digital components (AND, OR, NAND, NOR, XOR, XNOR, Inverter), Probe for Analysis and annotation (Digital), Schematic connectors (Ground)**

**CIRCUIT:**

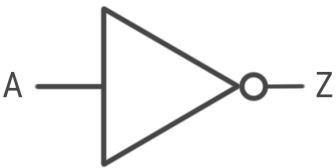
AND GATE OR GATE

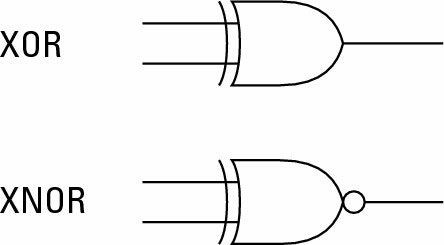


NAND GATE NOR GATE



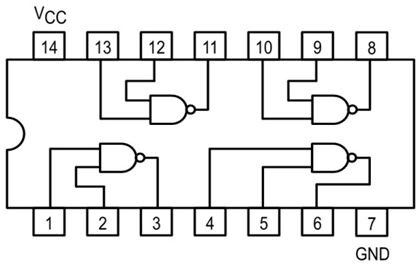
NOT GATE



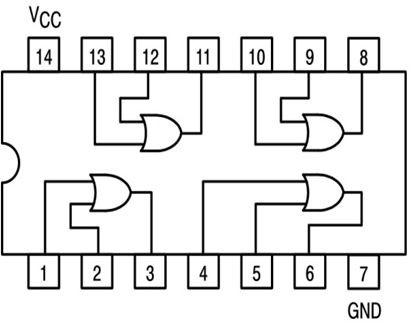


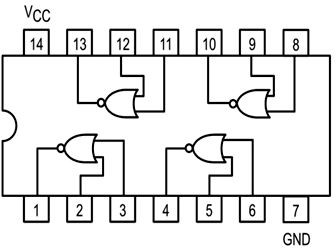
**PIN – DIAGRAM:**

# AND GATE

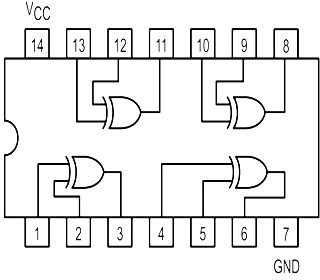
**NAND GATE**

**OR GATE**

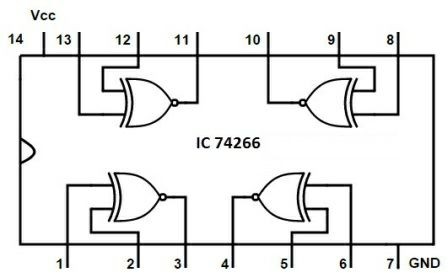


**NOR GATE**

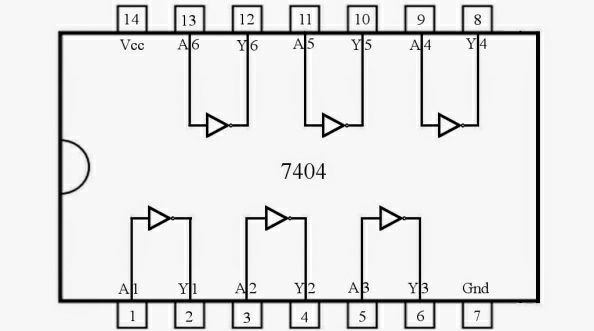
**XOR GATE**

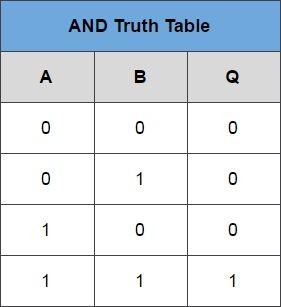
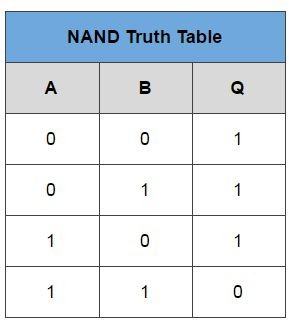
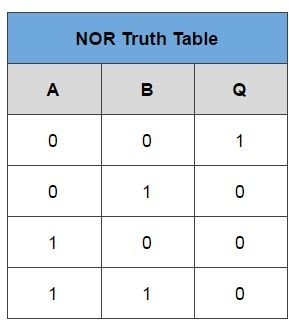


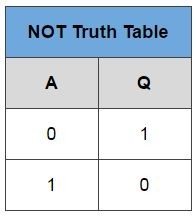
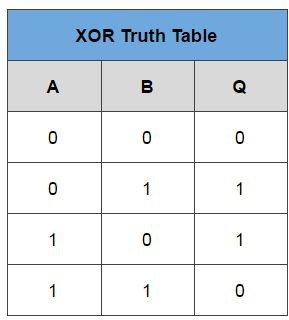
**XNOR GATE**

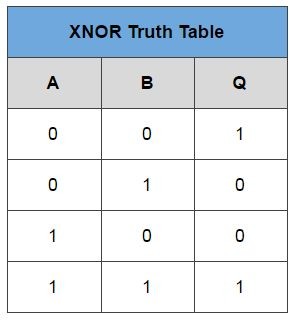
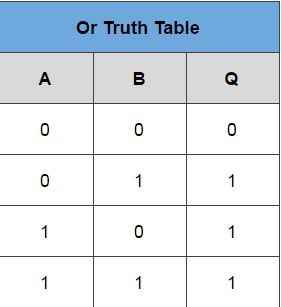


**NOT GATE**



**TRUTH TABLE****S**



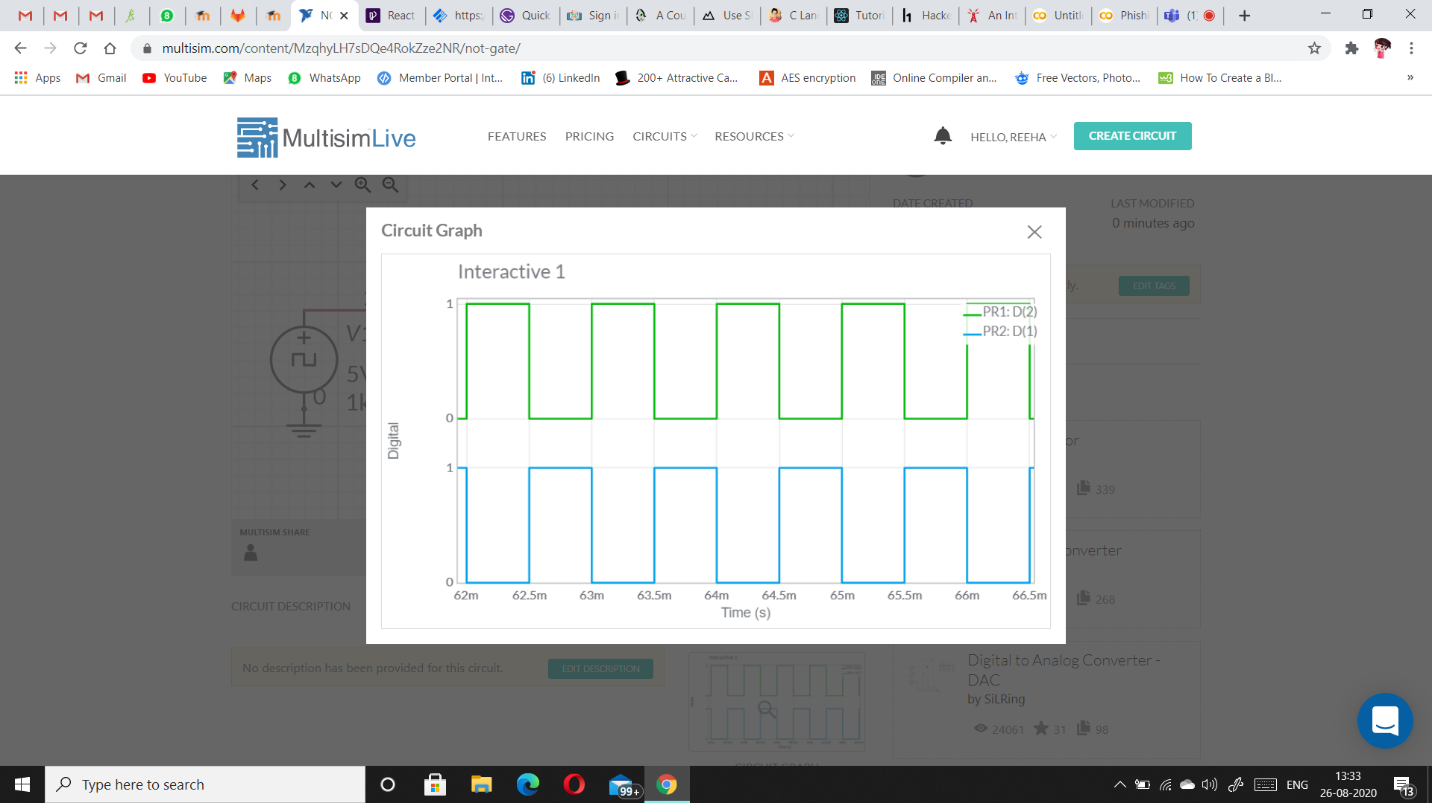
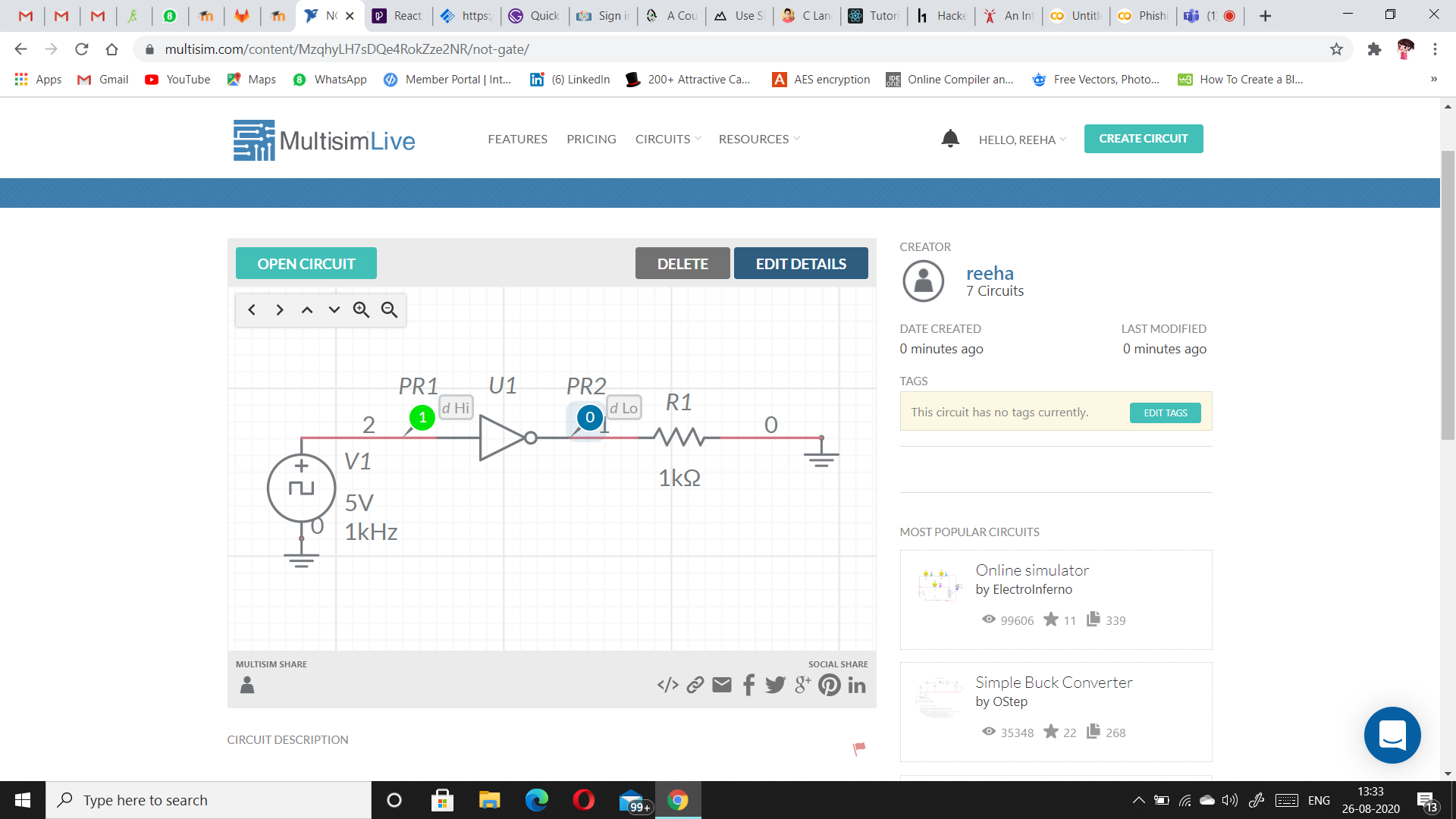
**THEORY:** Logic gates are electronic circuits which perform logical operations on one or more inputs to produce a signal output. There are 7 logic gates. These include the AND, NAND, OR, NOR, XOR, XNOR and NOT.

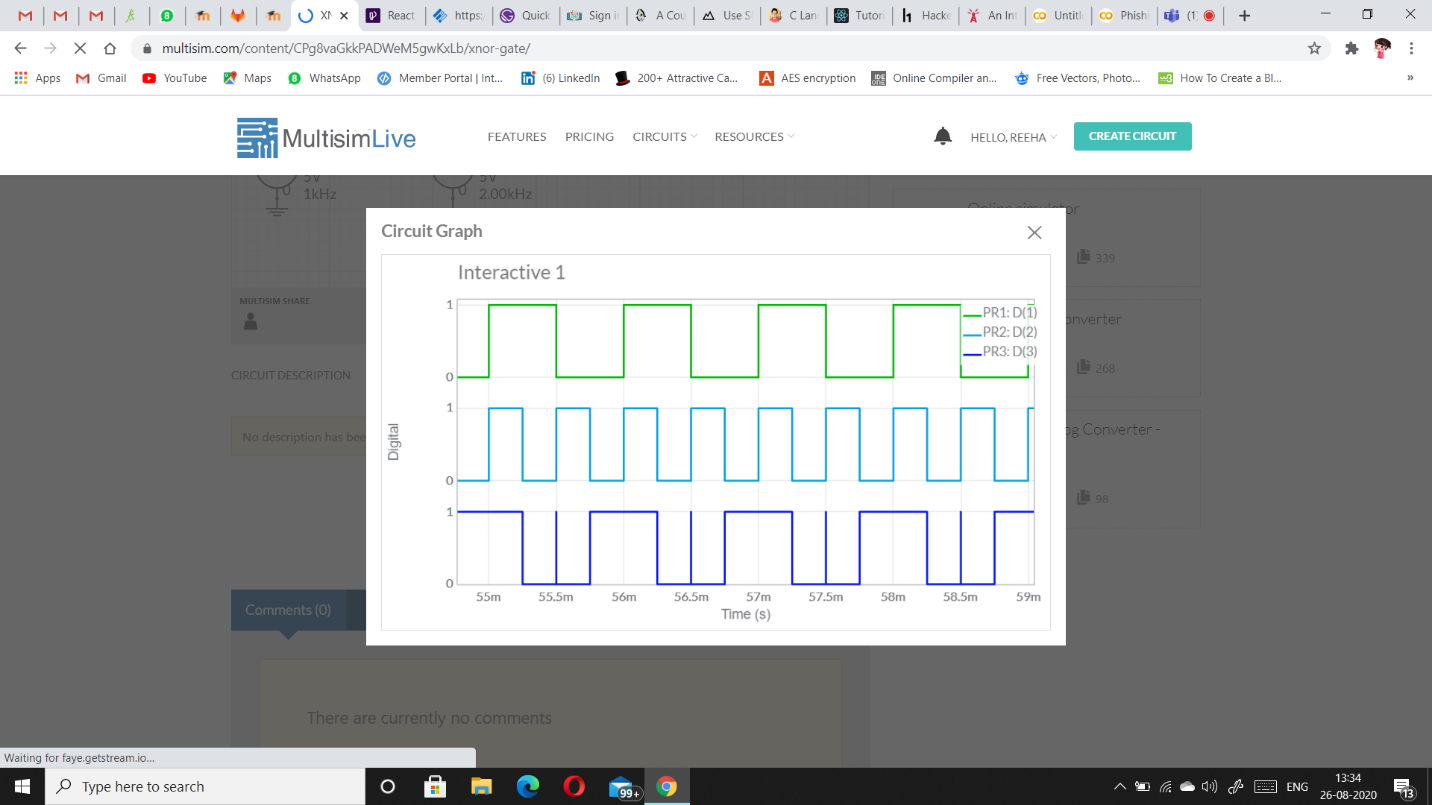
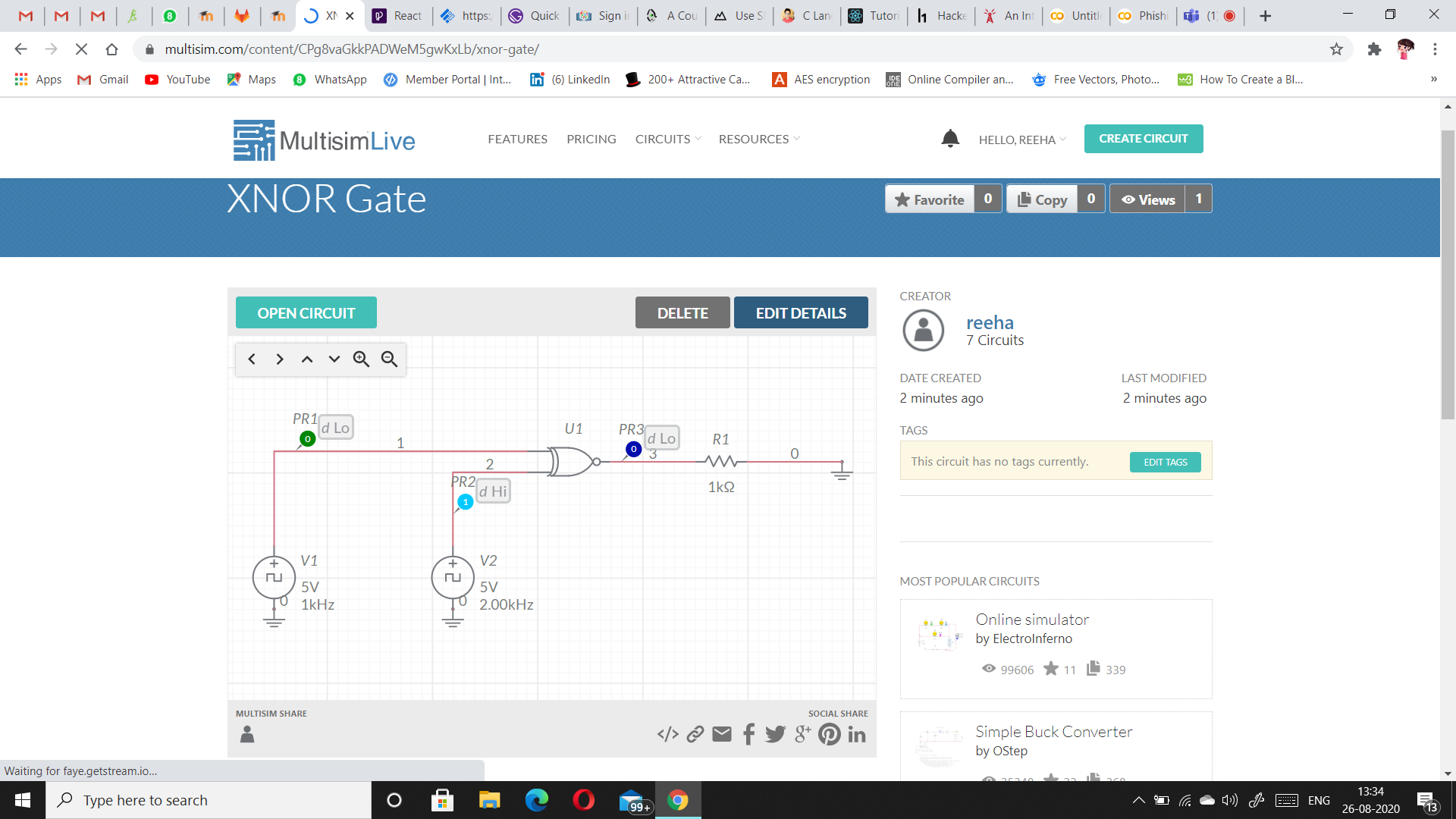
# PROCEDURE (MULTISIM):

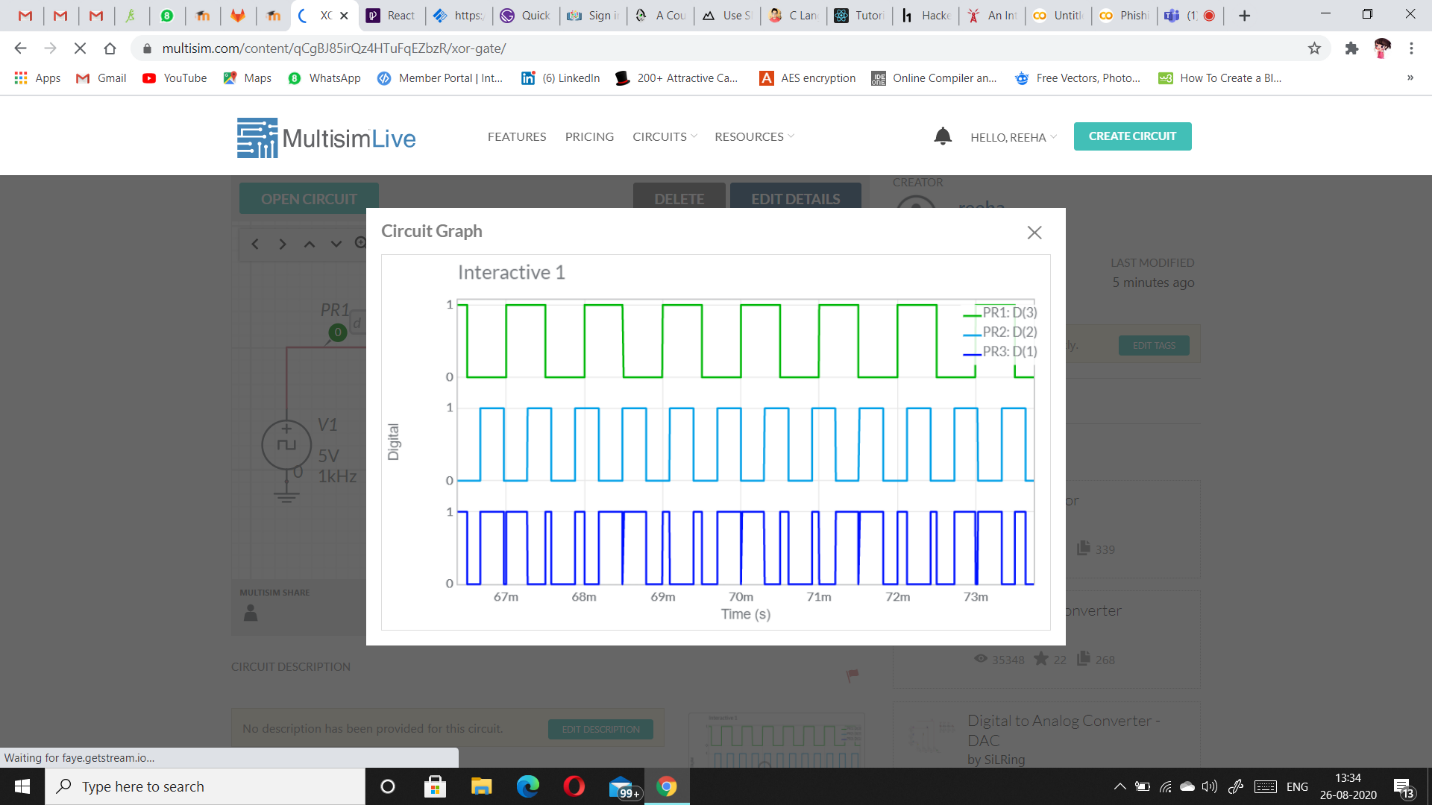
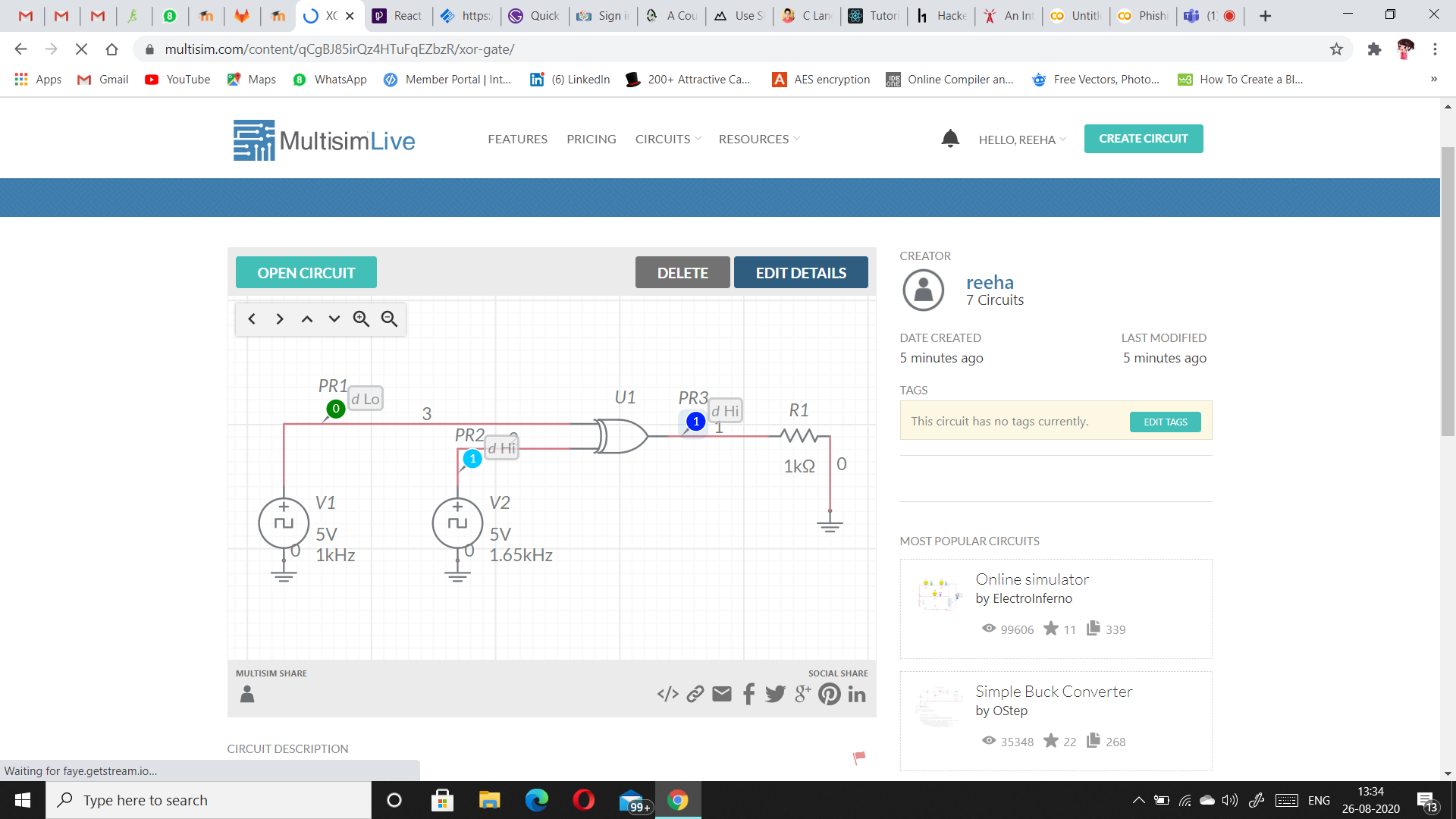
* Make the circuits shown as shown in the figures.
* Select the required components (gates, resistor, voltage sources (Clock Voltage) and ground symbols from the tool bar on the left.
* Ground both the voltage sources (clock Voltages) and then connect them to the input terminal of the gate.
* Connect the output terminal to 1 k ohm resistor and ground it.

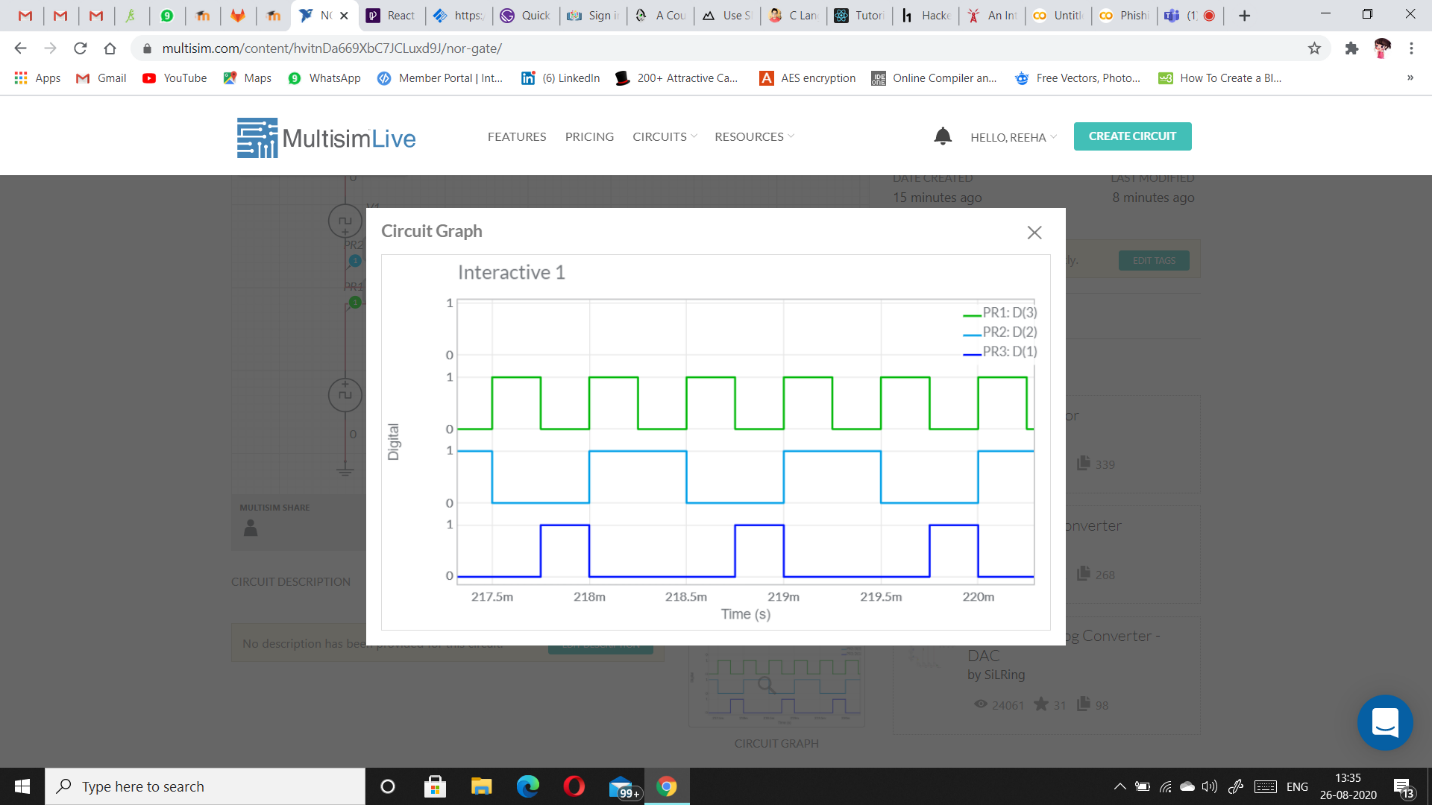
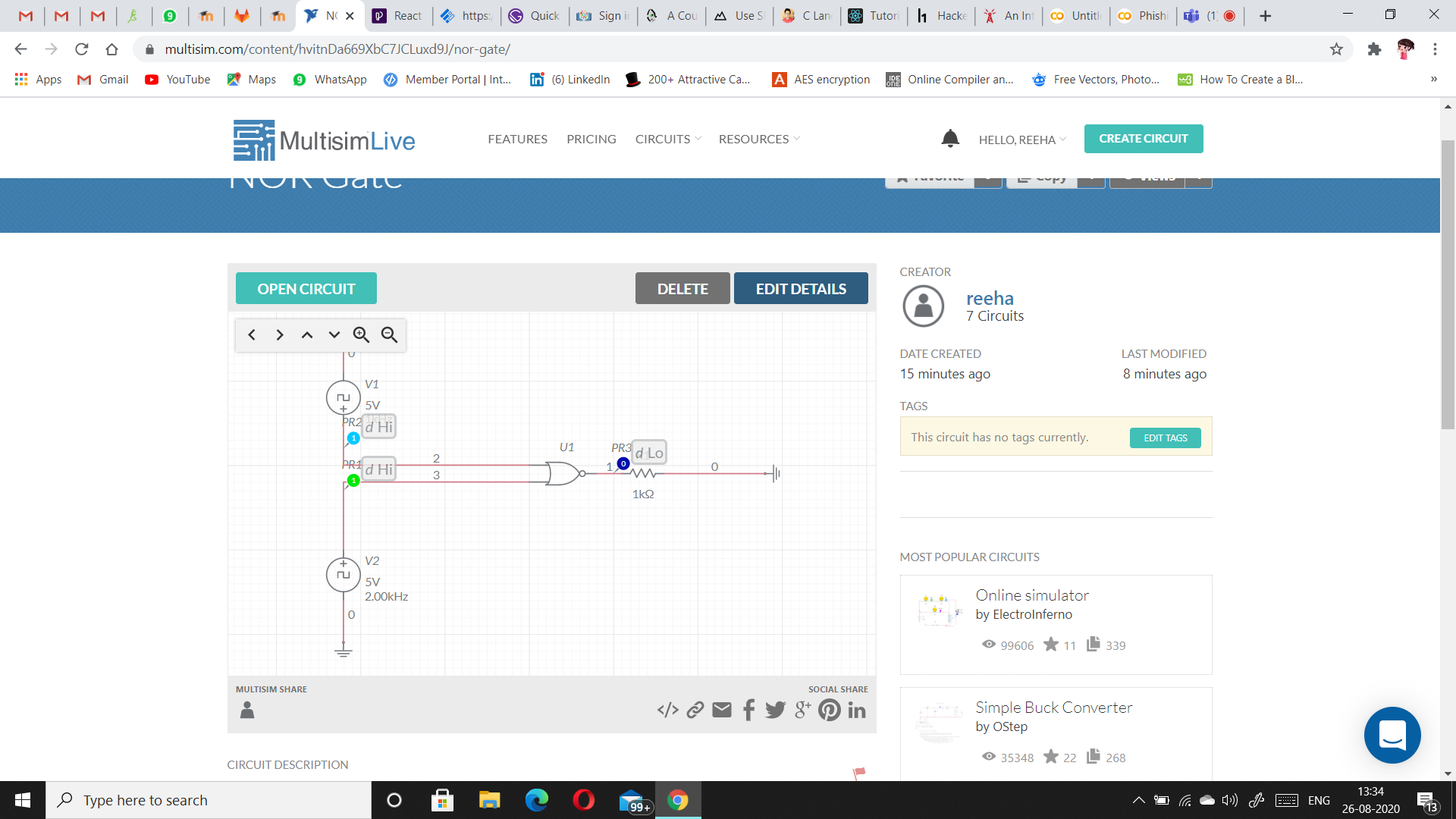
**Precautions:**

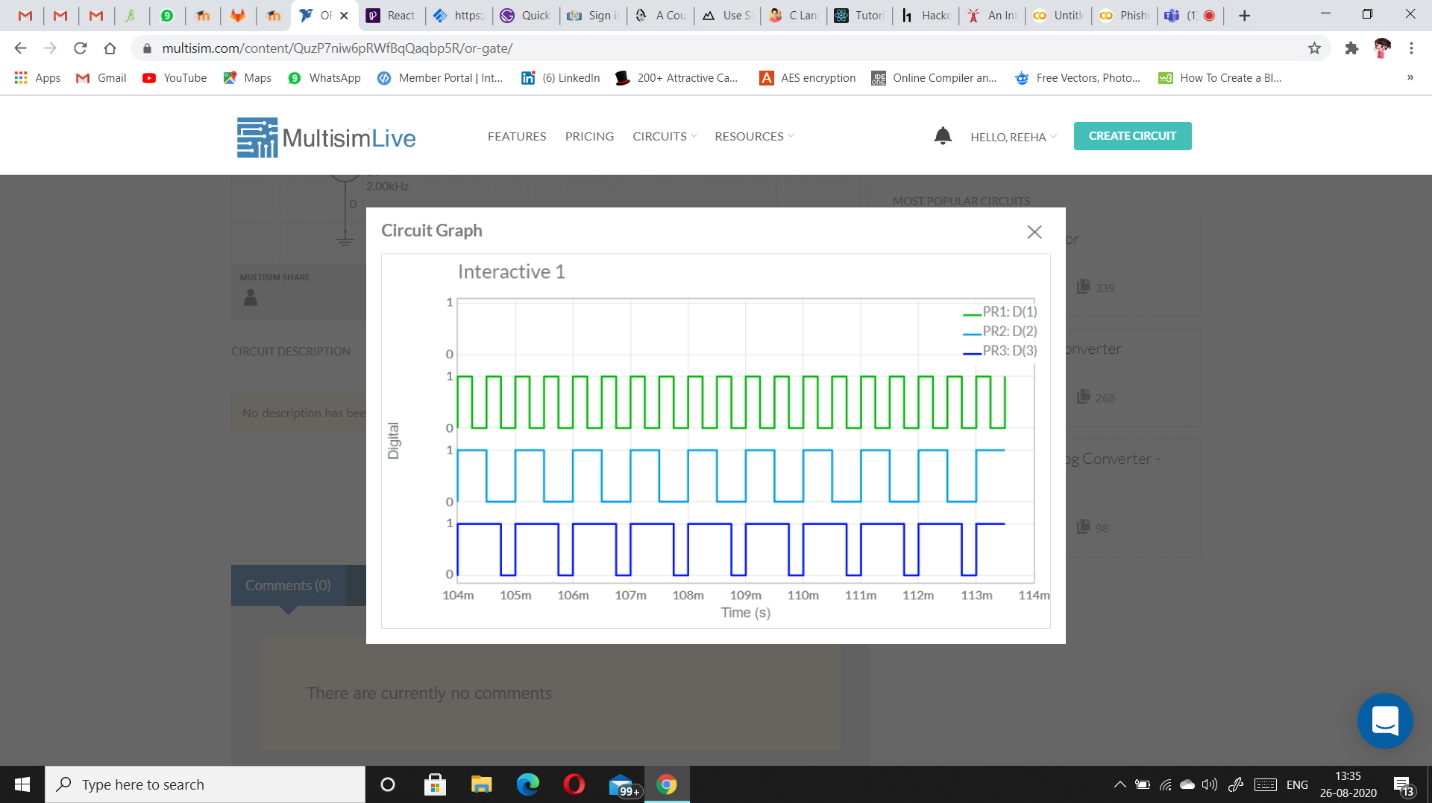
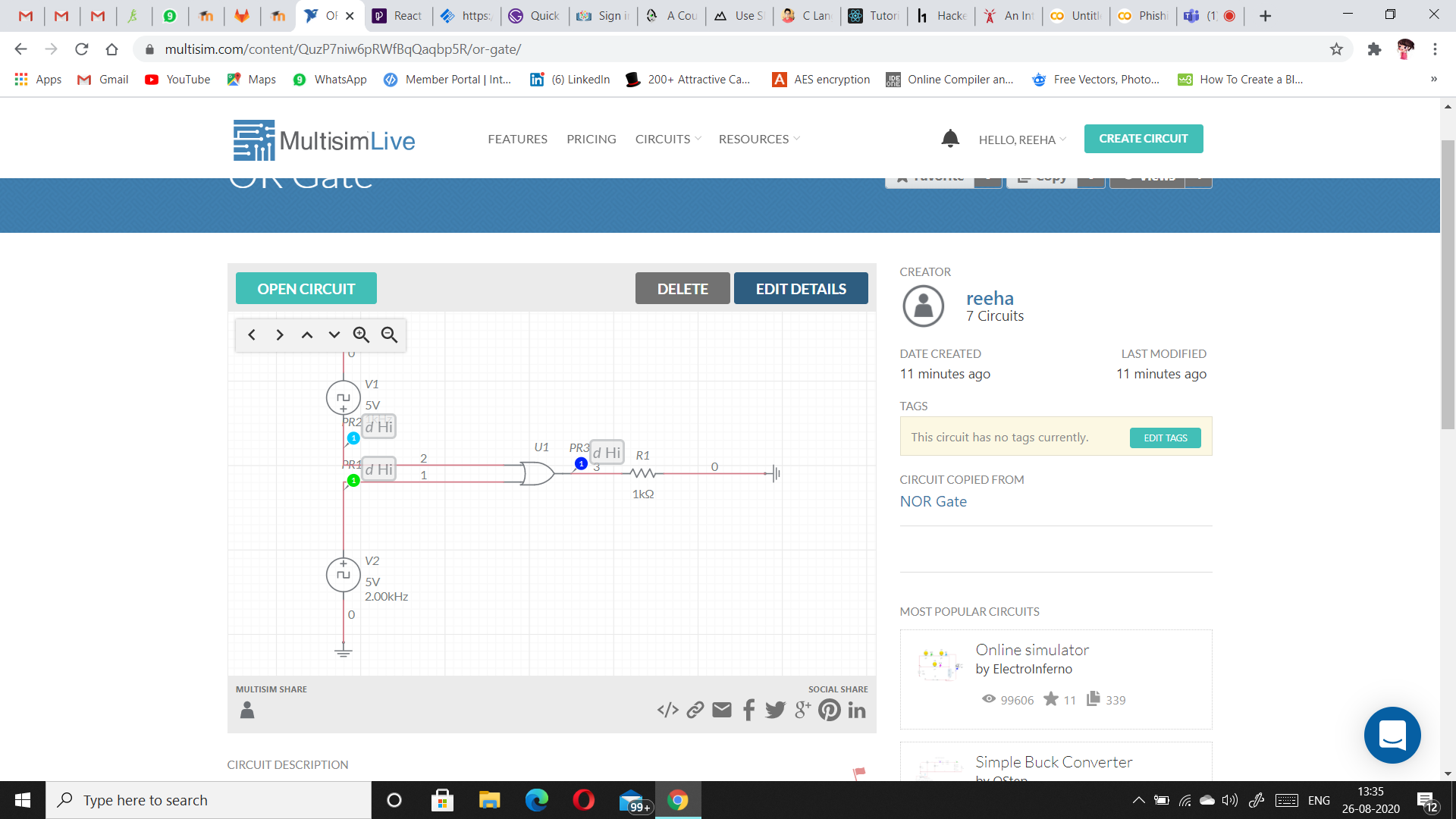
* Power supply should not exceed 5V.
* All the connections should be tight.
* Components should be tested before the practical.

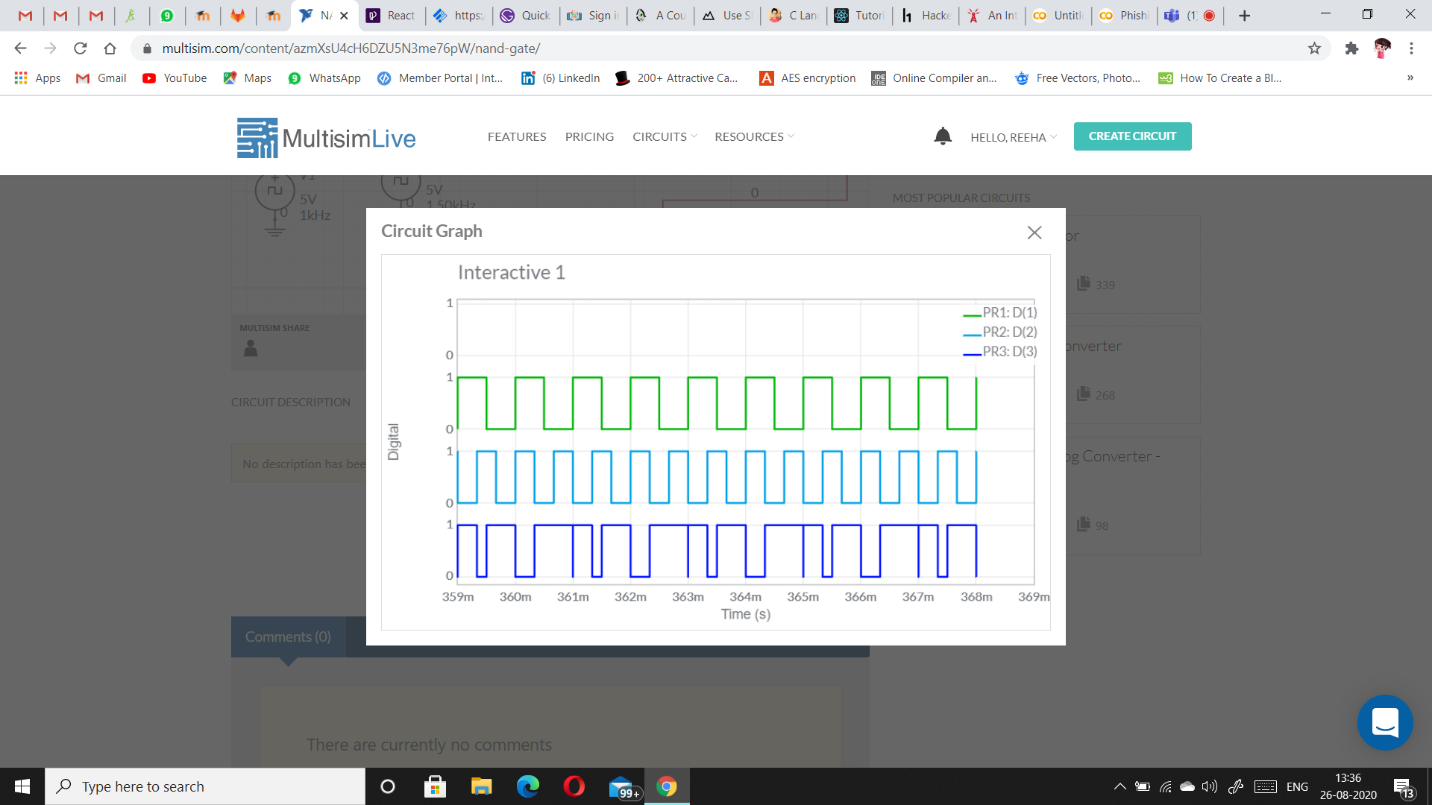
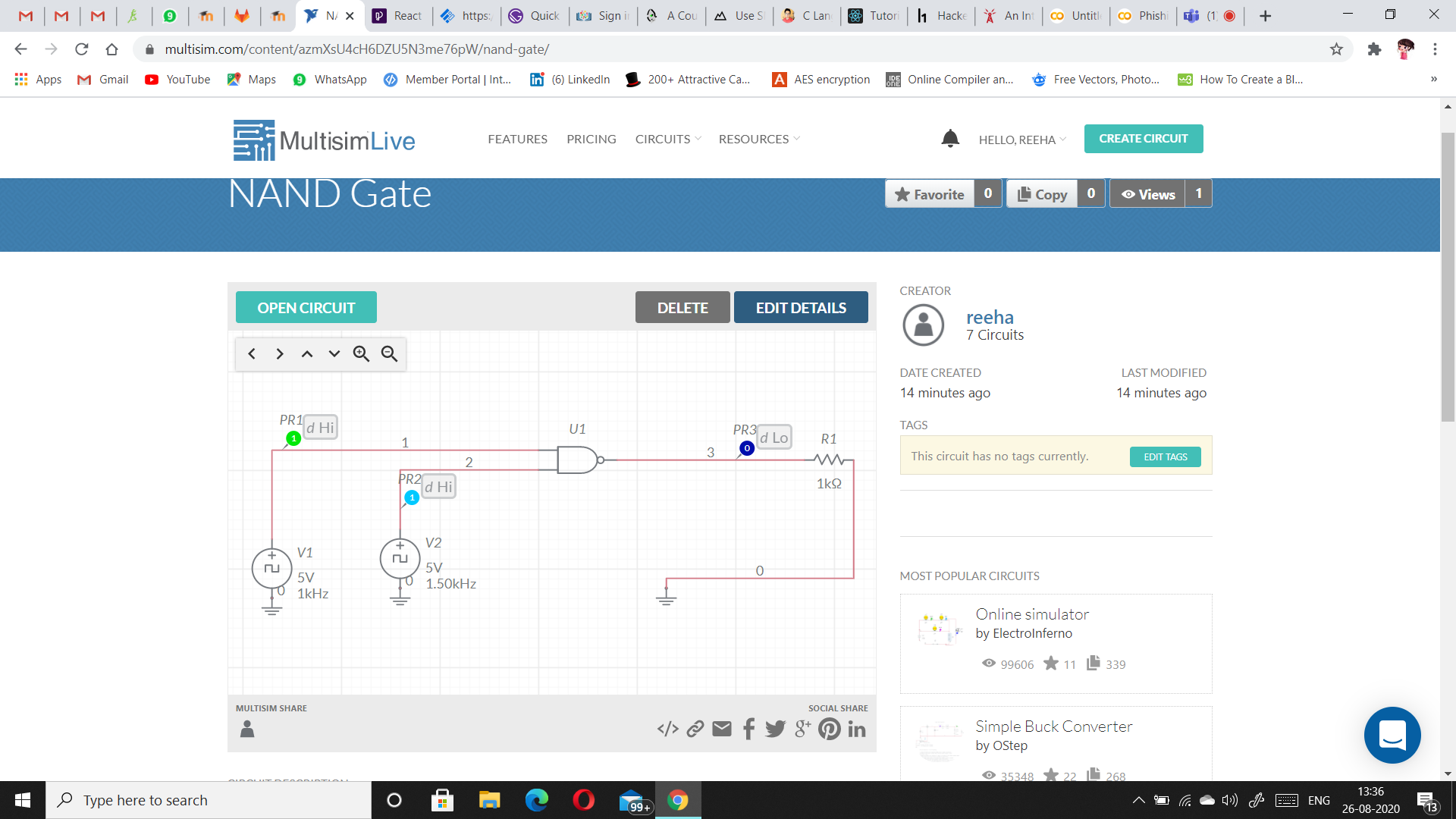
**NOT GATE**

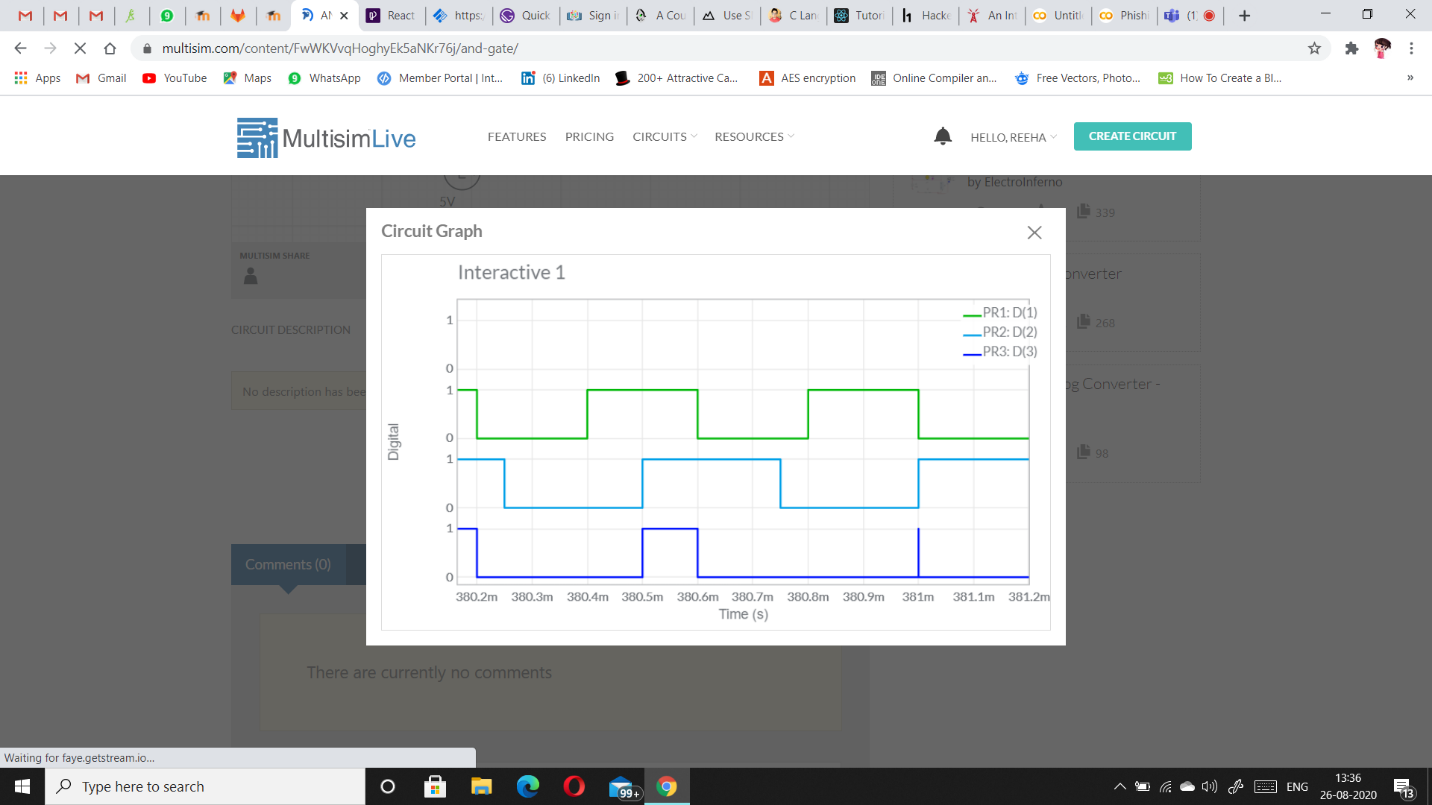
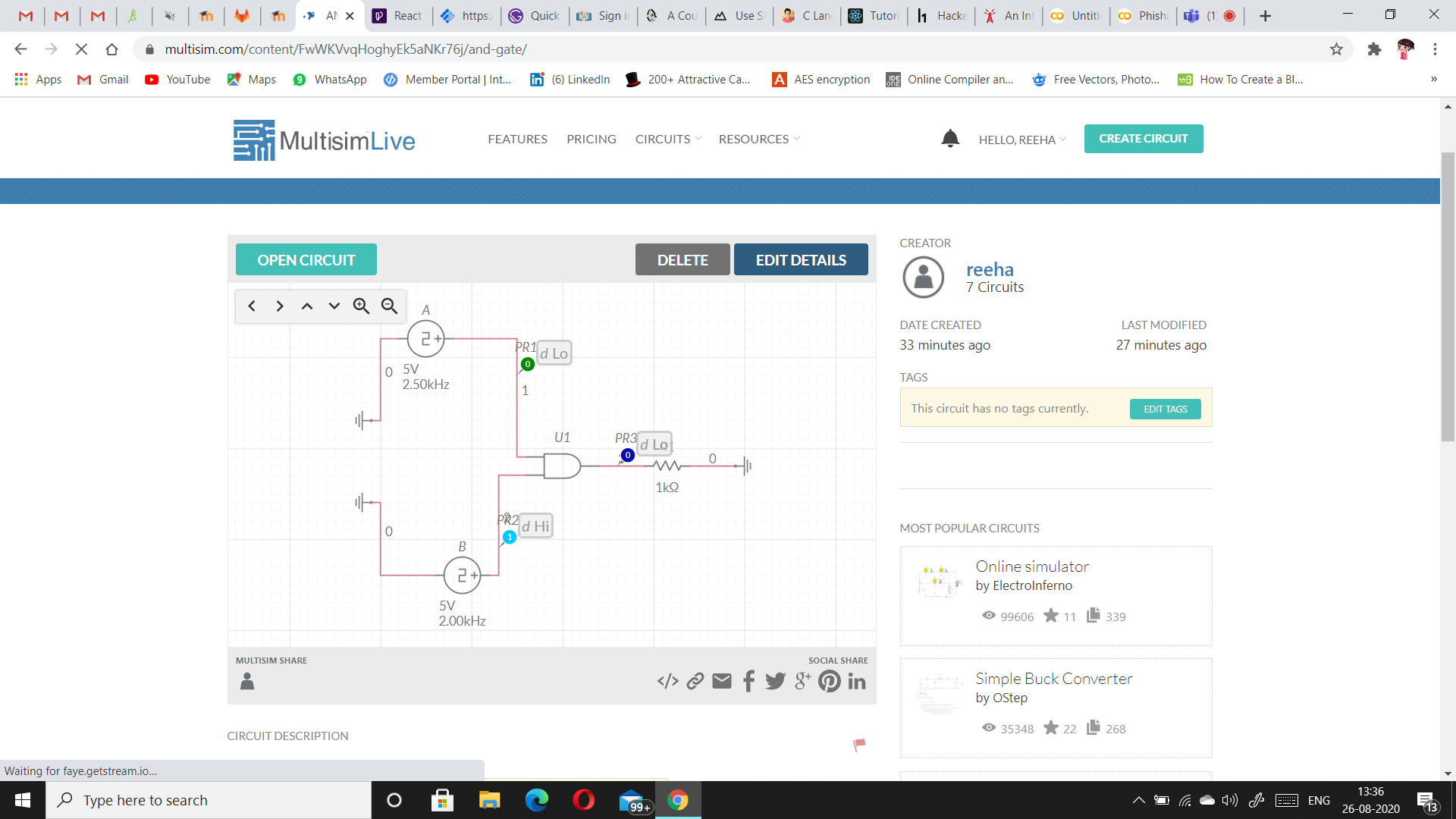
**XNOR GATE**

**XOR GATE**

**NOR GATE**

**OR GATE**

**NAND GATE**

**AND GATE**